UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/560,634	12/13/2005	Cornelis Adrianus Henricus Antonius Mutsaers	NL 030673	6812

24737 7590 04/29/2008
PHILIPS INTELLECTUAL PROPERTY & STANDARDS
P.O. BOX 3001
BRIARCLIFF MANOR, NY 10510

EXAMINER	
RALEIGH, DONALD L	
ART UNIT	PAPER NUMBER
2879	
MAIL DATE	DELIVERY MODE
04/29/2008	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/560,634	MUTSAERS, CORNELIS ADRIANUS HENRICUS AN	
	Examiner	Art Unit	
	DONALD L. RALEIGH	2879	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 January 2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1 and 3-17* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1 and 3-17* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *12/13/2005*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

The Amendment, filed on January 28, 2008 has been entered and acknowledged by the Examiner.

Cancellation of claim 2 has been entered.

Claims 1, and 3-17 are pending in the instant application.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1 and 3-17 are rejected under 35 U.S.C. 102(b) as being anticipated by Ghosh (US PGPub. 2001/0052752 A1).

Regarding Claim 1, Ghosh discloses a barrier laminate (Fig. 5) including barrier(21)and planarisation materials (Page 3 [0032] lines 3-4 teaches that this layer is a polymer. Page 4 [0037], lines 4-5 teaches that parylene is a preferred polymer and lines 6-8 teaches that Parylene helps cover defects and pinholes , i.e. constitutes a planarisation material), for use with a device layer (in Figure 3, elements (3) are the device layers) comprising: a device layer (3) and at least one discontinuous layer of a planarisation material(21)(Figure 3 shows the planarization material separated by oxide material (22), external to the device layer within a stack including the device layer (the

planarization layer is external to the device layer) , wherein the at least one discontinuous layer is divided into unconnected areas distributed along a plane wherein the unconnected areas are separated by regions of a barrier material (Figure 3 shows this and the barrier material is (22), and wherein the barrier material (22) separating the unconnected areas is external to the device layer(3) (Figure 3 shows this), which layer is divided into unconnected areas distributed along the plane. (Figure 3, shows the individual device layers unconnected along the plane).

Regarding Claim 3, Ghosh discloses wherein said planarisation material is an organic material. (Page 3 [0032] lines 3-4 teach that the 1st encapsulation layer may is formed of a polymer. Page 4, [0037] teaches that parylene is a preferred polymer. Page 4, [0037] lines 6-8 teaches that Parylene helps cover defects and pinholes , i.e. constitutes a planarisation material. Page 4 [0037]; chemical diagrams show that Parylene is organic (contains Carbon-Hydrogen bond (CH_2))

Regarding Claim 4, Ghosh discloses wherein said planarisation material is a combination of organic and inorganic materials. (Page 4, [0037], chemical diagrams show that Parylene C & D contains Carbon-Hydrogen bonds (CH_2) ,which is organic and Chlorine (Cl) which is inorganic.)

Regarding Claim 5, Ghosh discloses wherein said barrier material is an inorganic material. (Both of the layers (21) and (22) can be considered as barrier layers. The second encapsulation layer (22), Page 3 [0032], lines 15-16 is formed of an oxide layer.

Page 4, [0036], lines 5-9 teaches that a suitable material would be SiO_2, which is inorganic.)

Regarding Claim 6, Ghosh discloses wherein said regions of a barrier material forms a checked pattern. (Figure 5 shows a checked pattern of a barrier material (21) exposing parts of the substrate)(Paragraph [0032], lines 17-19)

Regarding Claim 7, Ghosh discloses further comprising at least one continuous layer of a barrier material. (Page 3 [0032], lines 17-19 teaches that barrier layer (22) covers layer (21) and the substrate).

Regarding Claim 8, Ghosh discloses wherein said discontinuous layer is arranged between two continuous layers of a barrier material.(Page 3, [0028], lines 8-11 teaches that the top layer of the OLED stack is a barrier layer of ITO. Although, inventor does not specify that this layer is continuous across the substrate; the substrate layer beneath the OLED stack is obviously continuous and presents a barrier layer sandwiching the 1st encapsulation layer (21) and the 2nd encapsulation layer(22)).

Regarding Claim 9, Ghosh discloses further comprising at least one continuous layer of a planarisation material.(Page.3, [0032], lines 23-32 teaches an optional arrangement of Fig.5 with a 3rd encapsulation layer (23) formed of a polymer that provides chemical protection. Page 4, [0037] teaches that parylene is a polymer that provides such protection. Additionally, Page 3 [0032], lines 31-32 teaches that an

additional SiO_2 layer can be added on layer (23) and Page 4, [0037] teaches that these oxide layers need to be protected with parylene , which is a planarisation material.

Regarding Claim 10, Ghosh discloses wherein said planarisation material is a polymeric material. (Page 4 [0037] teaches that Parylene is a suitable polymer for the planarisation layer. (It covers defects and pinholes , which is what a planarisation material is used for.)

Regarding Claim 11, Ghosh discloses wherein said planarisation material is selected from the group consisting of parylene, acrylates, epoxides, urethanes, spin-on dielectrics, and siloxanes. (Page 4 [0037], parylene)

Regarding Claim 12, Ghosh discloses wherein said barrier material is selected from the group consisting of are SiO_2, SiC, Si_3N_4, TiO_2 HfO_2, Y_2O_3, Ta_2O_3, and Al_2O_3. (Page 4, [0036], lines 5-9, which is used for the 2nd encapsulation (barrier) layer (22) . Page 3, [0032], lines 15-17).

Regarding Claim 13, Ghosh discloses the use of a barrier laminate that is an oxygen and/or water impermeable film. (Page 4, [0038], lines 1-3 teaches that Parylene C is low in oxygen permeability and moisture vapor transmission.)

Regarding Claim 14 , Ghosh discloses a method for the manufacture of a discontinuous layer (21) in a barrier laminate (21 and parylene) for use with a device layer comprising:

- depositing a continuous layer of a planarisation material,

- (Page.3, [0032], lines 23-32 teaches an optional arrangement of Fig.5 with a 3rd encapsulation layer (23) formed of a polymer that provides chemical protection. Page 4, [0037] teaches that parylene is a polymer that provides such protection. Additionally, Page 3 [0032], lines 31-32 teaches that an additional SiO_2 layer can be added on layer (23) and Page 4, [0037] teaches that these oxide layers need to be protected with parylene , which is a planarisation material).

- removing regions of said layer of a planarisation material and filling said regions with a barrier material

- (Fig.5, shows portions of layer (21) removed to expose the substrate. Page 3, [0032], lines 3-6) and filling said regions with a barrier material .

- (Page 3 [0032], lines 17-19 teaches the 2nd encapsulation (barrier (oxide)) layer (22) completely covering the first barrier layer (21) and the exposed substrate., i.e. filling in the exposed regions with barrier material).

- to form a barrier laminate layer external to the device layer (22 and 21 are external to the device layer) within a stack including the device layer such that the barrier material filling said regions is external to the device layer.(22 is external to the device layer (3)(Figure 3))

Regarding Claim 15, Ghosh discloses a method for the manufacture of a discontinuous layer (Fig.5 (21)) in a barrier laminate (21 and parylene) for use with a device layer comprising:

depositing a patterned layer of a planarisation material (parylene), whereby regions where no planarisation material is deposited are formed, (Fig.5 shows exposed regions of the substrate that layer (21) containing the parylene does not cover) and filling said regions with a barrier material.

- (Page 3 [0032], lines 17-19 teaches the 2nd encapsulation (barrier) layer (22) completely covering the first barrier layer (21) and the exposed substrate., i.e. filling in the exposed regions with barrier material)
- to form a barrier laminate layer external to the device layer within a stack including the device layer such that the barrier material filling said regions is external to the device layer.

Regarding Claim 16, Ghosh discloses wherein said filling of said regions with a barrier material is performed simultaneously as the deposition of a continuous layer of a barrier material on said discontinuous layer. (The deposition of the 2nd barrier layer (22) would fill in the exposed regions and simultaneously create a continuous barrier layer across the entire substrate and OEL portions).

Regarding Claim 17, Ghosh discloses a barrier laminate wherein the at least one discontinuous layer is positioned over active layers of an electronic device and is ,

among layers of the laminate including planarisation material, closest to the active layers of said electronic device.

Response to Arguments

Applicant's arguments filed January 28, 2008 have been fully considered but they are not persuasive.

Regarding Claim 1, applicant's statement is that Ghosh fails to disclose or render obvious a barrier laminate with barrier materials separating unconnected portions of planarization material that are external to a device layer.

As shown in Figure 3 of Ghosh , the barrier material (22 (oxide)) separates unconnected portions of planarization material (21) that are external to a device layer (3)(See Paragraph [0032]).

The rejections of Claims 3-13, which depend upon claim 1, stand as originally proposed.

Regarding Claims 14 and 15, applicant's statement is that Ghosh fails to disclose or render obvious a barrier laminate layer external to the device layer within a stack including the device layer such that the barrier material filling said regions is external to the device layer.

As shown in Figure 3 of Ghosh, a barrier laminate (21 and 22) is external to device layer (3) and the barrier material (both 21 and 22) is external to the device layer (3).

The rejections of Claim 16-17, which depend upon Claim 15 stand as originally proposed.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Examiner's note: Examiner has cited particular columns and line numbers in the references as applied to the claims above for the convenience of the applicant. Although the specified citations are representative of the teachings of the art and are applied to the specific limitations within the individual claim, other passages and figures may apply as well. It is respectfully requested from the applicant in preparing responses, to fully consider the references in entirety as potentially teaching all or part

of the claimed invention, as well as the context of the passage as taught by the prior art or disclosed by the examiner.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to DONALD L. RALEIGH whose telephone number is (571)270-3407. The examiner can normally be reached on Monday-Friday 7:30AM to 5:00PM EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nimesh Patel can be reached on 571-272-2457. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Donald L Raleigh/
Examiner, Art Unit 2879

/Nimeshkumar Patel/
Supervisory Patent Examiner, Art Unit 2879